Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

21. (Previously presented): An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected;

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus; and

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus, said analysis unit including:

a storage device for storing therein inspection data produced by said inspection apparatus and position information of regions of a circuit pattern to be formed on said object;

a calculation device for identifying particles and pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities for said particles and said pattern defects positioned in said regions based on their sizes; and

a selection device for selecting particles or pattern defects whose calculated failure probabilities are greater than or equal to a predetermined threshold.

22. (**Withdrawn**): An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected;

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus; and

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus comprising:

a storage device for storing therein inspection data produced by said inspection apparatus and position information of regions of one or more edge portions of a circuit pattern to be formed on said object; and

a selection device for selecting those of said particles and said pattern defects that are outside of said regions.

23. (**Withdrawn**): An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected;

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus; and

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus comprising:

a storage device for storing therein inspection data produced by said inspection apparatus and position information of one or more regions of a circuit pattern to be formed on said object; and

a selection device for selecting those of said particles and pattern defects being positioned in predetermined regions of said one or more regions.

24. (Previously presented): The inspection system according to claim 21, wherein said regions are circuit blocks as formed within an LSI chip.

25. (**Withdrawn**): The inspection system according to claim 22, wherein said edge portions constitute portions of circuit blocks as formed within an LSI chip.

26. (**Withdrawn**): The inspection system according to claim 23, wherein said regions are circuit blocks as formed within an LSI chip.

27. (Previously presented): The inspection system according to claim 21, further comprising a simulation device for generating virtual defects at random positions with respect to circuit graphics obtainable from mask layout data forming said circuit pattern, and

computing said failure probabilities from connection relationships of said circuit graphics and said defects.

28. (Previously presented): The inspection system according to claim 21, wherein said position information of said regions is generated from mask layout data forming an LSI chip.

29. **(Withdrawn)**: The inspection system according to claim 22, wherein said position information of said edge portions is generated from mask layout data forming an LSI chip.

30. **(Withdrawn)**: The inspection system according to claim 23, wherein said position information of said regions is generated from mask layout data forming an LSI chip.

31. (Previously presented): The inspection system according to claim 24, wherein said position information of said circuit blocks is generated from mask layout data forming an LSI chip.

32. **(Withdrawn)**: The inspection system according to claim 25, wherein said position information of said circuit blocks s is generated from mask layout data forming an LSI chip.

33. **(Withdrawn)**: The inspection system according to claim 26, wherein said position information of said circuit blocks is generated from mask layout data forming an LSI chip.

34. **(Withdrawn)**: An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected;

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus; and

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus comprising:

a storage device for storing therein inspection data produced by said inspection apparatus and layout information of said object to be inspected; and

a selection device for selecting particles or pattern defects from said inspection data based on said layout information.

35. (**Withdrawn**): The inspection system according to claim 34, wherein said layout information is position information as to a region within an LSI chip to be formed on said object to be inspected.

36. (Previously presented): A method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer, said circuit patterns constituting a plurality of semiconductor chips;

an inspection step for detecting positions and sizes of particles or pattern defects of said wafer;

identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns that constitute one of said semiconductor chips;

a calculation step for calculating failure probabilities based on sizes of said pattern defects in said region;

an extraction step for extracting positions of said particles or said pattern defects with calculated failure probabilities greater than or equal to a predefined threshold; and

producing images of said particles or said pattern defects extracted at said extraction step.

37. (Previously presented): A method for manufacturing semiconductor devices according to claim 36, wherein said regions are circuit blocks within an LSI chip.

38. (Previously presented): A method for manufacturing semiconductor devices according to claim 37, wherein said LSI chip is a system LSI and said circuit blocks include memory portions and logic portions.

39. **(Withdrawn)**: A method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer, said circuit patterns constituting circuitry of one or more LSI chips;

an inspection step for producing first information relating to positions and sizes of particles or pattern defects of said wafer;

an extraction step for extracting data of the particles or the pattern defects from said first information based on layout information of one of said LSI chips; and

producing images of said particles or said pattern defects extracted at said extraction step.

40. **(Withdrawn)**: A method for manufacturing semiconductor devices according to claim 39, wherein said layout information is position information of one or more regions as designed within an LSI chip, and said step of extracting includes identifying those particles or pattern defects located in predetermined regions of said one or more regions.

41. **(Withdrawn)**: A method for manufacturing semiconductor devices according to claim 39, wherein said layout information is position information of one or more edge portions of regions as designed within an LSI chip, and said step of extracting includes identifying those particles or pattern defects located in regions exclusive of said one or more edge portions.